



Intel[®] 82801EB I/O Controller Hub 5 (ICH5) / Intel[®] 82801ER I/O Controller Hub 5 R (ICH5R)

Specification Update

November 2007

Notice: The ICH5/ICH5R product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 252517-028



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The Intel® 82801EB I/O Controller Hub 5 (ICH5) / Intel® 82801ER I/O Controller Hub 5 RAID (ICH5R) component may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Revision History

Revision	Description	Date
-001	Initial Release.	April 2003
-002	Modified 1.5 V Voltage Margin Erratum and Markings Table	May 2003
-003	Added: Errata: SATA Transport Layer Erratum, Alternate Status Erratum, ASF Decode Erratum, PCI Non-linear Addressing Erratum Specification Clarification: SMBus Byte Done Status Clarification Documentation Changes: Figure 2 Note Addition, Table 177 Correction, LAN_RST# Correction, T173 Correction	June 2003
-004	Added: Documentation Changes: PME Wake Doc Change	July 2003
-005	Added: Erratum: SATA Signal Voltage Level Erratum, SATA COMINIT/COMWAKE Detection Erratum, MW DMA Mode-1 Tdh Erratum Specification Changes: SATA Partial and Slumber State Not Supported, RAID 1 Support Specification Clarification: PERR# Implementation Documentation Changes: PCIRST# Description Change, APM I/O Decode Correction, SATA PCS Register Changes, Memory Map Table Change	August 2003
-006	Added: Erratum: SATA Speed Negotiation Erratum Documentation Change: SMBus Host_Busy Bit Correction	September 2003
-007	Added: Specification Clarifications: SATA Behavior Spec Clarification, Test Mode Entrance Clarification Documentation Changes: GEN_CNTL Register Correction	October 2003
-008	Added: Specification Clarification: GPIO SMI/SCI Mapping Documentation Changes: Assorted Corrections, GPIO SMI/SCI Mapping	November 2003
-009	Added: Errata: LPC Starvation Erratum Specification Clarification: SERR# Figure Corrections	January, 2004
-010	Added: Documentation Change TCO_STS Correction	February, 2004
-011	Added: Vol2/Iol2 Specification Change and SATA MSI Support Specification Change.	March, 2004
-012	Added: Errata: USB Buffer Overrun Erratum Specification Changes: Absolute Maximum Ratings Specification Clarifications: Port 63/65/67 Clarification, GPI ACPI Clarification	May, 2004
-013	Added: Specification Clarification: USBCONFIGFLAG Clarification	June 2004



Revision	Description	Date
-014	Added: Erratum: SATA Swap Bay Device Detection	July 2004
-015	Added: Specification Changes: RTC Circuit Change Specification Clarifications: CTS Clarification	August 2004
-016	Added: Erratum: USB2 Incorrect Periodic Frame List Pointer Fetch	September 2004
-017	Added: Markings: Added SL73Z Documentation Change: SRS/PRS Bit Reference Correction	October 2004
-018	Added: Specification Clarifications: EDD (Execute Device Diagnostics) Command Completion Clarification Document Changes: GEN2_DEC Correction, GPIO_USE_SEL2 Correction	November 2004
-019	Added: Specification Changes: 8-t176 Change	December 2004
-020	Added: Specification Clarifications: 12-GPIO Note Change	January 2005
-021	Added: Specification Clarifications: 13-GPI_ROUT Clarification	February 2005
-022	Added: Errata: 14-Full-speed USB ISOC End of Packet Specification Clarifications: 14-LPC Cycle Clarification	March 2005
-023	Added: Specification Clarifications: 15-HPET TIMERn_32MODE_CNF Documentation Changes: 19-GP_LVL Default	April 2005
-024	Added: Documentation Changes: 20-IDE MSE Bit Modified: Specification Clarification: 15-HPET Timern_32MODE_CNF	May 2005
-025	Added: Documentation Change: 21-USB Port Number Documentation Corrections.	November 2005
-026	Added: Specification Changes: 9-t170 Change	March 2006
-027	High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level	September 2007
-028	Added: Specification Change: 10-Remove Support for USB Wake From S5	November 2007

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Note: This document contains information related to the ICH5/ICH5R components and their respective datasheet document. Refer to the **Affected Docs** section of each item to determine which component or document is affected by that particular item.

Affected Documents/Related Documents

Title	Document Number
<i>Intel® 82801EB I/O Controller Hub 5 (ICH5) / Intel® 82801ER I/O Controller Hub 5 R (ICH5R) Datasheet</i>	252516-001

Nomenclature

Errata are design defects or errors. Errata may cause the ICH5/ICH5R's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the Intel® I/O Controller Hub5 (ICH5)/Intel® I/O Controller Hub5 RAID (ICH5R). Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or

(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

Errata

Number	Steppings		Status	ERRATA
	A2	A3		
1	X		Fixed	1.5 V Voltage Margin
2	X	X	No Fix	SATA Transport Layer Erratum
3	X	X	No Fix	Alternate Status Erratum
4	X	X	No Fix	ASF Decode Erratum
5	X	X	No Fix	PCI Non-linear Addressing Erratum
6	X	X	No Fix	SATA Signal Voltage Level Erratum
7	X	X	No Fix	SATA COMINIT/COMWAKE Detection Erratum
8	X	X	No Fix	MW DMA Mode-1 Tdh Erratum
9	X	X	No Fix	SATA Speed Negotiation Erratum
10	X	X	No Fix	LPC Starvation Erratum
11	X	X	No Fix	USB Buffer Overrun Erratum
12	X	X	No Fix	SATA Swap Bay Device Detection
13	X	X	No Fix	USB2 Incorrect Periodic Frame List Pointer Fetch
14	X	X	No Fix	Full-speed USB ISOC End of Packet
15	X	X	No Fix	High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Specification Changes

Number	SPECIFICATION CHANGES
1	VOL8 Change
2	SATA Partial and Slumber State Not Supported
3	RAID 1 Support
4	Vol2/!ol2 Specification Change
5	SATA MSI Support
6	Absolute Maximum Ratings Addition
7	RTC Circuit Change
8	t176 Change
9	t170 Change
10	Removing Support for USB Wake from S5

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
1	SMBus Byte Done Status Clarification
2	PERR# Implementation
3	SATA Behavior Spec Clarification

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
4	Test Mode Entrance Clarification
5	GPIO SMI/SCI Mapping
6	SERR# Figure Corrections
7	Port 63/65/67 Clarification
8	GPI ACPI Clarification
9	USB CONFIGFLAG Clarification
10	CTS Clarification
11	EDD (Execute Device Diagnostics) Command Completion Clarification
12	GPIO Note Change
13	GPI_ROUT Clarification
14	LPC Cycle Clarification
15	HPET TIMERn_32MODE_CNF

Documentation Changes

Number	DOCUMENTATION CHANGES
1	PCI Device Revision ID
2	Figure 2 Note Addition
3	Table 177 Correction
4	LAN_RST# Correction
5	T173 Correction
6	PME Wake Doc Change
7	PCIRST# Description Change
8	APM I/O Decode Correction
9	SATA PCS Register Changes
10	Memory Map Table Change
11	SMBus Host_Busy Bit Correction
12	GEN_CNTL Register Correction
13	Assorted Corrections
14	GPIO SMI/SCI Mapping
15	TCO_STS Correction
16	SRS/PRS Bit Reference Correction
17	GEN2_DEC Correction
18	GPIO_USE_SEL2 Correction
19	GP_LVL Default
20	IDE MSE Bit
21	USB Port Number Documentation Corrections.

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Identification Information

Markings

Intel® ICH5/ICH5R Stepping	S-Spec	Top Marking	Notes
A2	N/A	82801EB QE41 ES	Engineering Sample (82801EB ICH5)
A2	N/A	82801ER QE42 ES	Engineering Sample (82801ER ICH5R)
A2	SL6TN	82801EB SL6TN	Production (82801EB ICH5)
A3	N/A	82801EB QE51 ES	Engineering Sample (82801EB ICH5)
A3	SL73C	82801EB SL73C	Production (82801EB ICH5)
A3	SL73Z	82801EB SL73Z	Production (82801EB ICH5)
A3	N/A	82801ER QE52 ES	Engineering Sample (82801ER ICH5R)
A3	SL73D	82801ER SL73D	Production (82801ER ICH5R)
A3	SL742	82801ER SL742	Production (82801ER ICH5R)

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Errata

1. 1.5 V Voltage Margin

Problem: If the Vcc1_5 Core power well and the VccSus1_5 power well diverge towards their outer boundaries of their $\pm 5\%$ tolerance levels, the high-speed USB 2.0 circuitry may not synchronize accurately.

Implication: High-speed USB 2.0 devices may disconnect.

Workaround: A board workaround has been developed to reduce the ability of the voltage rails to diverge.

- Note: This workaround is not needed for A3 stepping.

- Contact appropriate Intel field representative if workaround details are needed.

Status: Fixed in the A3 step prior to volume production and launch. For steppings affected, see the *Summary Tables of Changes*.

2. SATA Transport Layer Erratum

Problem: ICH5 does not retry non-data FIS errors. SATA Specification Rev 1.0 implies that non-data FIS errors be retried via hardware.

Implication: None known. Non-data FIS errors will be retried via software (driver).

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

3. Alternate Status Erratum

Problem: In native mode IDE, when the Alternate Status Register for SATA device 1 is accessed and there is not a device connected, the register value is decoded as a 50h (device present) instead of 00h (device not present).

Implication: Warning message may occur in some Linux operating systems indicating a discrepancy between the Alt Status and the Status registers. Linux will use the correct Status register data and continue execution.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

4. ASF Decode Erratum

Problem: After receiving an ACK from a remote management console, the ICH5 ASF controller may, under certain circumstances, incorrectly decode the Remote Management and Control Protocol (RMCP) header. The incorrect decode may result in the ICH5 inappropriately sending an ACK to the management console.

Implication: None known.

The redundant ACK generated by the ICH5 will be ignored and dropped by the management console via the Intel management console software development kit available to developers.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

5. PCI Non-linear Addressing Erratum

Problem: If a PCI Memory Read Multiple or Memory Read Line transaction falls at the last DW of a 32-byte cache line boundary and non-linear addressing (cache-line wrap mode) is used the ICH5 will pre-fetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent CPU cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

Implication: None known.

- System hang only seen in synthetic test environment.

- No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

6. SATA Signal Voltage Level Erratum

Problem: The ICH5 SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH5 Serial ATA (SATA) transmit signalling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 6.6.2 of SATA Specification, rev 1.0).

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

7. SATA COMINIT/COMWAKE Detection Erratum

Problem: During Out-Of-Band (OOB) sequencing, the ICH5 may detect COMINIT/COMWAKE when only 2 or 3 bursts of ALIGNs are received from the SATA device instead of the required 4 bursts as per the SATA 1.0 Specification.

Implication: None, due to how the ICH5 handles subsequent ALIGNs.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

8. MW DMA Mode-1 Tdh Erratum

Problem: Data hold time of MW DMA Mode-1 writes may not meet ATA specification.

Implication: None known.

Workaround: Program the controller to PIO Mode-4 instead.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

9. SATA Speed Negotiation Erratum

Problem: During the SATA device - ICH5 initialization sequence (which occurs each time the SATA port is enabled), if a 3 Gb/s SATA device attempts to complete the sequence with 3 Gb/s ALIGN primitives, the ICH5 may prematurely respond (by sending valid 1.5 Gb/s ALIGN primitives) to the device. A device may misinterpret this as a proper 3 Gb/s response and continue transactions at 3 Gb/s resulting in a failure to establish communication.

Implication: If a SATA device initially attempts to communicate at 3 Gb/s, then the ICH5 and the drive may fail to establish communication at any speed (fail to detect the device).

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

10. LPC Starvation Erratum

Problem: Latency issues on LPC may occur if a PCI bus master is performing large upstream bursts to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may get delayed until the PCI device completes its transaction and de-asserts its REQ#.

Implication: Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

11. USB Buffer Overrun Erratum

Problem: If a USB full speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20 uS of system latency) and the USB FIFO begins to empty during a 30 nS window immediately prior to the overrun event actually occurring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

Implication: Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behavior. There is no known exposure with real world applications.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

12. SATA Swap Bay Device Detection

Problem: During SATA swap bay operation with a slave device while a master is present, the slave device task file may stay at 00h if the slave device is not ready.

Note: This only applies when SATA is operating in combined mode.

Implication: Slave SATA device swapped may not be detected.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

13. USB2 Incorrect Periodic Frame List Pointer Fetch

Problem: The USB2 controller may fetch an incorrect periodic frame list pointer when the periodic activity is heavily scheduled and there are large latencies on descriptor requests to memory when running HS isochronous or interrupt traffic.

Note: This has only been reproduced in synthetic test environments.

Implication: There may be intermittent audio pops or lost video frames on USB2 HS devices when the system is heavily loaded in synthetic test environments.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

14. Full-speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

15. High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH5 may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

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Specification Changes

1. VOL8 Change

VOL8 specification is being changed from 0.05 V max at 0.5 mA IOL to .10V max at 1.0 mA IOL.

2. SATA Partial and Slumber State Not Supported

Section 5.17.4.2.1 (Partial and Slumber State Entry/Exit) is replaced with the following

5.17.4.2.1 Partial and Slumber State

The ICH5 SATA controller does not support partial or slumber state device transitions and does not issue any transitions as a host. Device initiated requests for a partial slumber transition will be NACKed by the SATA host controller.

3. RAID 1 Support

RAID Level 1 is supported in addition to RAID Level 0. The Features List and Section 5.17.3 are updated accordingly.

4. Vol2/IoI2 Specification Change

As indicated in Table 181 (DC Output Characteristics), Vol2 max is changed from 0.25(V_CPU_IO) to 0.25 V and IoI2 is increased from 1.5 mA to 2.5 mA.

5. SATA MSI Support

Section 5.17.5 (SATA Interrupts) indicates that SATA Message Signalled Interrupts (MSIs) are supported when they are not. This section is replaced with the following:

Table 79 summarizes interrupt behavior. In the table “bits” refers to the four possible interrupt bits in I/O space, which are: BMIS[P].PRDIS (offset 02h, bit-7), BMIS[P].Interrupt (offset 02h, bit-2), BMIS[S].PRDIS (offset 0Ah, bit-7), and BMIS[S].Interrupt (offset 0Ah, bit-2).

Table 79. SATA PCI IRQ Actions

Interrupt Register	Wire-Mode Action
All bits are 0	Wire Inactive
One or more bits set to 1	Wire Active
One or more bits set to 1, new bit gets set to 1	Wire Active
One or more bits set to 1, software clears some (but not all) bits	Wire Active
One or more bits set to 1, software clears all bits	Wire Inactive
Software clears one or more bits, and one or more bits are set simultaneously	Wire Active

6. Absolute Maximum Ratings Addition

A new section, Absolute Maximum Ratings (19.2) is added after section 19.1 as indicated (this renumbers sections 19.2 & 19.3 to 19.3 & 19.4):

19.2 Absolute Maximum Ratings

Parameter	Maximum Limits
Voltage on Any 3.3 V Pin with respect to Ground	-0.5 to Vcc3_3 + 0.5 V
Voltage on Any 5 V Tolerant Pin with respect to Ground (V5REF=5 V)	-0.5 to V5REF + 0.5 V
1.5 V Supply Voltage with respect to Vss	-0.5 to +2.1 V
3.3 V Supply Voltage with respect to Vss	-0.5 to +4.6 V
5.0 V Supply Voltage (V5REF) with respect to Vss	-0.5 to + 5.5 V

7. RTC Circuit Change

Figure 2 (Example External RTC Circuit) is renamed to “External RTC Circuit”. Additionally, the resistor and capacitor value on RTCRST# is changed from 180 kΩ to 20 kΩ and from 0.1 μF to 1.0 μF.

8. t176 Change

Symbol t176 in Table 194 is changed to remove the reference to VRMPWRGD. This specification relates to the PCI 2.3 requirements, of which VRMPWRGD does not apply. “VRMPWRGD” is deleted from the reference figures 20, and 21. “V_CPU_IO is removed from the reference figure 20.

Additionally, a new timing is added t176a

Sym	Parameter	Min	Max	Units	Notes	Fig
t176a	V_CPU_IO to VRMPWRGD	10		ms		

9. t170 Change

The minimum value of t170 in Table 194 is changed to 18ms as indicated below:

Sym	Parameter	Min	Max	Units	Notes	Fig
t170	VccRTC active to RTCRST# inactive	18		ms		20

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10. Removing Support for USB Wake from S5

Support for USB wake from S5 is removed from Datasheet as indicated below.

a. Update Intel® ICH5 Features page of the Datasheet as follows:

USB 2.0

- New: Includes 4 UHCI Host Controllers, increasing the number of external ports to eight
- Includes 1 EHCI Host Controllers that supports all eight ports
- Includes 1 USB 2.0 High-speed Debug Port
- Supports wake-up from sleeping states **S1-S4**
- Supports legacy Keyboard/Mouse software

b. Update Table 5-31 as follows:

Table 64. Causes of Wake Events

Cause	States Can Wake From	How Enabled
USB	S1-S4	Set USB1_EN, USB 2_EN, USB3_EN, and USB4_EN bits in GPE0_EN register

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Specification Clarification

1. SMBus Byte Done Status Clarification

The note associated with the Byte Done Status bit in Section 14.2.1 Host Status is being replaced with the following:

Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit-1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, another interrupt may be generated if the INTR bit is set. Thus, for a block message of n-bytes, the Intel® ICH5 may generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.

2. PERR# Implementation

The ICH5 does not escalate a data parity mismatch reported by a PCI device (PERR#) across the PCI to PCI bridge. The PCI Specification or PCI to PCI bridge spec does not require PERR# escalation across the PCI to PCI bridge.

For certain applications, it may be desirable to generate an SMI or NMI upon PERR# assertion by a PCI device. The device/driver is expected to handle such situations by retrying the transactions or escalating to the OS via device driver. Alternatively, external circuitry can be added to platforms to drive SMI or NMI upon PERR# assertion.

3. SATA Behavior Spec Clarification

The following note is added to Section 5.17.2 of the datasheet.

Note: If communication between the SATA controller and the SATA device has been completely lost (for example, SATA cable is disconnected from the motherboard or device, SATA device misbehavior, and so on), the loss of communication may be interpreted as a surprise removal by the controller.

4. Test Mode Entrance Clarification

The following note is added to Section 21.1 of the datasheet:

Note: Wait 150 ms after RTCRST# rising edge before attempting to use the test mode.

5. GPIO SMI/SCI Mapping

The following note is added to the description for GPIIn_STS (in GPE0_STS) and GPIIn_EN (in GPE0_EN):

Note: Mapping is as follows: bit-31 corresponds to GPI:[15] and bit-16 corresponds to GPI:[0].

The following note is added to the descriptions for Alternate GPI SMI Enable (in ALT_GP_SMI_EN) and Alternate GPI SMI Status (in ALT_GP_SMI_STS):

Note: Mapping is as follows: bit-15 corresponds to GPI:[15] and bit-0 corresponds to GPI:[0].

6. SERR# Figure Correction

The Figures 5-7 are inaccurate and is being replaced with the following figures:

Figure 5.

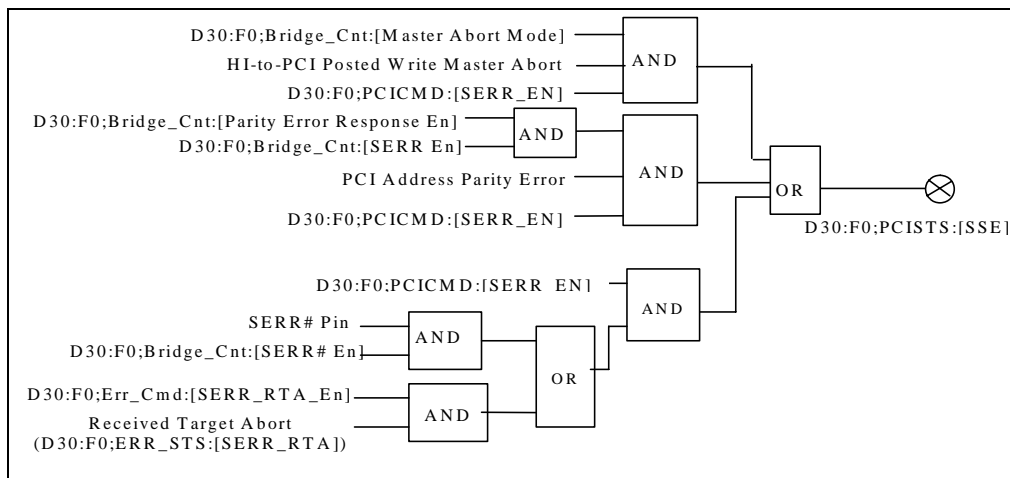


Figure 6.

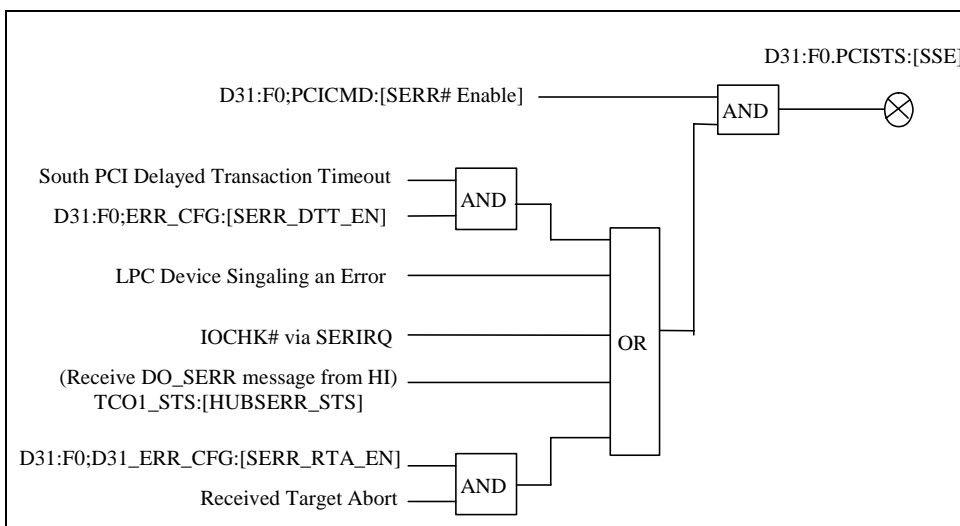
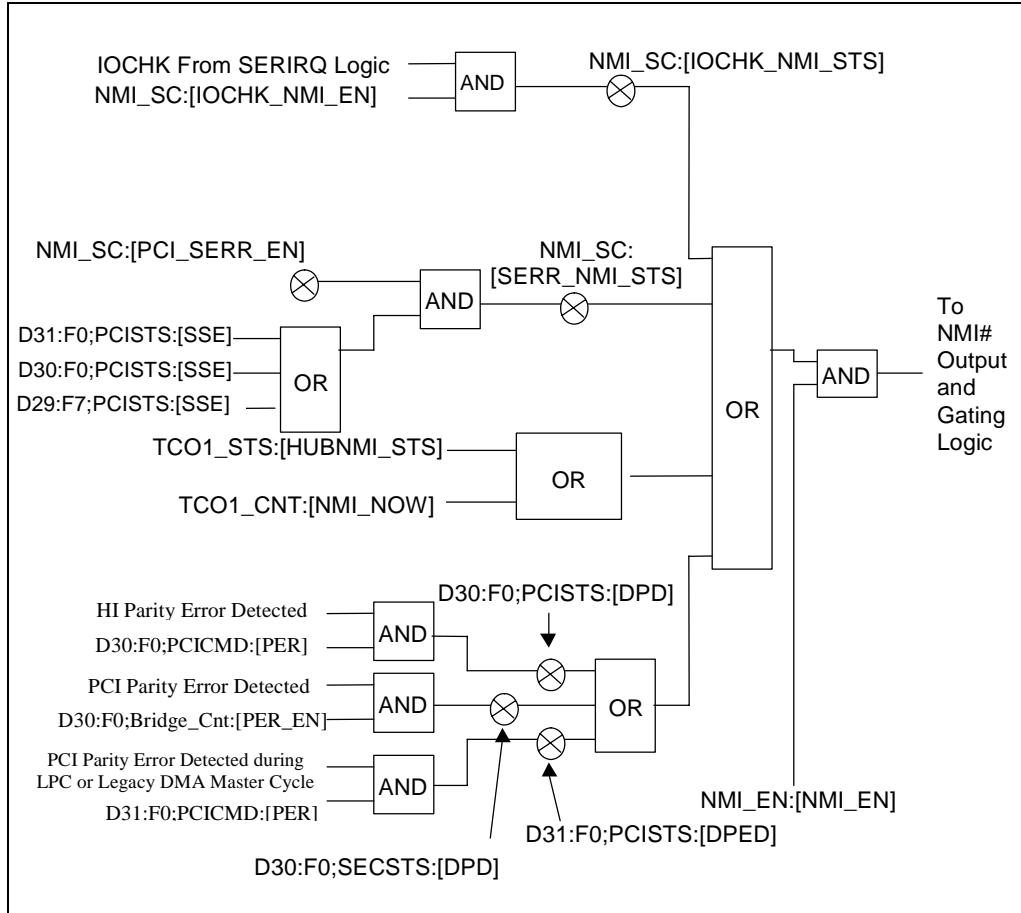


Figure 7.



7. Port 63/65/67 Clarification

Table 131 (Fixed I/O Ranges Decoded by Intel(R) ICH5) incorrectly lists ports 63, 65 and 67 as addresses decoded by the processor I/F. These addresses are entirely removed from this table.

8. GPI ACPI Clarification

Section 5.13.7.3 incorrectly indicates that some GPIs, specifically GPI[7:0] are not ACPI complaint when they actually are. The paragraph above Table 65 and Table 65 are changed as indicated:

“It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from an S1 state. Table 65 summarizes the use of GPIs as wake events.”

Table 65. GPI Wake Events

GPI	Power Well	Wake From	Notes
GPI[7:0]	Core	S1	ACPI Compliant
GPI[13:11, 8]	Resume	S1-S5	ACPI Compliant

9. USB CONFIGFLAG Clarification

The paragraph associated with Section 13.2.12 (CONFIGFLAG - Configure Flag Register) is completely replaced with the paragraph below:

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

10. CTS Clarification

The following note is added to the CTS bit description (Section 9.8.2):

Note: The CF9h reset in this description refers to CF9h type core well reset which includes SYS_RESET#, PWROK/VRMPWRGD low, SMBus hard reset and TCO timeout. This type of reset will clear the CTS bit.

11. EDD (Execute Device Diagnostics) Command Completion Clarification

The following applies to Section 5.17.1.1 (Standard ATA Emulation):

The ICH5 will assert INTR when the master device completes the EDD command regardless of the command completion status of the slave device. If the master completes EDD first, an INTR is generated and BSY will remain '1' until the slave completes the command. If the slave completes EDD first, BSY will be '0' when the master completes the EDD command and asserts INTR. Software must wait for busy to clear ('0') before completing an EDD command, as required by the ATA5 through ATA7 (T13) industry specifications.

12. GPIO Note Change

The following is added to Note 1 of Table-74; "and may be subject to further design constraints."

13. GPI_ROUT Clarification

Add to the GPI_ROUT register bit description (Section 9.8.7 bits 1:0): "Software must set this bit field to generate the appropriate type of system interrupt, depending on how the SCI_EN bit is set. For example, if the SCI_EN bit is set, then this field must be programmed to 00b or 10b. If the SCI_EN bit is cleared, then this field must be programmed to 00b or 01b. Software must also update this field if the SCI_EN bit is changed."

14. LPC Cycle Clarification

The following changes are made to Table 33 LPC Cycle Types Supported in section 5.4.1.1:

- “See Note 1” is removed from the comment column for both I/O Read and I/O Write cycle types. §
- “See Note 1 is added to the comment column for both Memory Read and Memory Write cycle types.

15. HPET TIMERn_32MODE_CNF

The description of TIMERn_32MODE_CNF (section 17.5) is replaced as follows:

Bit	Description
8	<p>Timer n 32-bit Mode (TIMERn_32MODE_CNF) - R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of atomic 64-bit operations to the timer. This bit is only relevant if the timer is operating in 64-bit mode in which case that timer can be forced to 32-bit mode by setting this bit. When Timer 0 is switched to 32-bit mode, the upper 32 bits are loaded with 0's which will remain when the timer is switched back to 64-bit mode. If the timer is not in 64-bit mode, then this bit will always be read as 0 and writes will have no effect.</p> <p>Timer 0: Read/Write (default 0). 0 = 64-bit, 1=32-bit.</p> <p>Timers 1/2: Hardwired to 0. Writes have no effect since these timers are 32-bit only.</p>

§

Documentation Changes

1. PCI Device Revision ID

PCI Revision ID Register Values (PCI Offset 08h) for all ICH5/ICH5R functions are shown below.

This information is not found in the datasheet. This is the standard reference document.

Device Function	Description	Intel® ICH5 Dev ID	ICH5 A2/A3 Rev ID	Comments
D30, F0	PCI-to-PCI Bridge	244Eh	C2h	ICH5 and ICH5R
D31, F0	PCI-to-LPC Bridge	24D0h	02h	ICH5 and ICH5R
D31, F1	IDE	24DBh	02h	ICH5 and ICH5R
D31, F2	SATA	24D1h	02h	ICH5 only
		24DFh	02h	ICH5R only
D31, F3	SMBus	24D3h	02h	ICH5 and ICH5R
D31, F5	AC97 Audio	24D5h	02h	ICH5 and ICH5R
D31, F6	AC97 Modem	24D6h	02h	ICH5 and ICH5R
D8, F0	LAN	1051h	82h	ICH5 and ICH5R, Note 1
D29, F0	USB UHCI #1	24D2h	02h	ICH5 and ICH5R
D29, F1	USB UHCI #2	24D4h	02h	ICH5 and ICH5R
D29, F2	USB UHCI #3	24D7h	02h	ICH5 and ICH5R
D29, F3	USB UHCI #4	24DEh	02h	ICH5 and ICH5R
D29, F7	USB EHCI	24DDh	02h	ICH5 and ICH5R

NOTE:

1. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 1051h is used. Refer to the ICH5 EEPROM Map and Programming Guide for LAN Device IDs.

2. Figure 2 Note Addition

The following note is added below Figure 2 for consistency with other requirements:

Note: Diodes must be Schottky

3. Table 177 Correction

Table 177 is replaced as follows:

Table 177. DC Current Characteristics

Power Plane	Maximum Power Consumption ⁽⁴⁾				
	S0	S1	S3	S4/S5	G3
Vcc1_5 Core	770 mA	201 mA	N/A	N/A	N/A
Vcc3_3 I/O	480 mA	1 mA	N/A	N/A	N/A
VccSus3_3 ⁽³⁾	360 mA	73 mA	73 mA	73 mA	N/A
VccRTC	N/A	N/A	N/A	N/A	6 μ A ^(1,2)
V_CPU_IO	2.5 mA	2.5 mA	N/A	N/A	N/A
V5REF	250 μ A	250 μ A	N/A	N/A	N/A
V5REF_Sus	200 μ A	200 μ A	200 μ A	200 μ A	N/A

NOTES:

1. Only the G3 state for this power well is shown to provide an estimate of battery life.
2. Icc(RTC) data is taken with VccRTC at 3.0V while the system is in a mechanical off (G3) state at room temperature.
3. Due to the integrated voltage regulator, VccSus1_5 is part of the VccSus3_3 power rail.
4. Icc data for Sx states is taken while the system is at nominal Vcc and at room temperature.

4. LAN_RST# Correction

The description for LAN_RST# in Section 2.11, Power Management Interface, Table 13 is being updated as follows:

Table 13. Power Management Interface Signals (partial)

Name	Type	Description
LAN_RST#	I	LAN Reset: When asserted, the internal LAN controller will be put into reset. This signal must be asserted at least 10 mS after the resume well power (VccSus3_3) is valid. When deasserted, this signal is an indication that the resume well power is stable.

5. T173 Correction

The parameter of T173 in Table 194 of Section 19.3 is being corrected as follows:

Table 194. Power Sequencing and Reset Signal Timings (partial)

Sym	Parameter	Min	Max	Units	Notes	Fig
t173	VccSus supplies active to LAN_RST# HIGH, RSMRST# HIGH	10	-	mS		20 21

6. PME Wake Doc Change

The following changes are made to Section 5.13.7.3: Table 64.

Note 1 is changed to “This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software or from a power failure.”

Note 3 is added: “This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software.”

The note associated with GPI:[0:n] is changed from Note 1 to Note 3.

The following changes are made to Section 5.13.7.4:

The last sentence of the third paragraph is changed to read: “There are four possible events that will wake the system after a power failure.

Add a fourth item: PME: PME_STS or PME_B0_STS, if enabled, will wake the system from S5 if S5 is entered from an AC power failure or if entered by a write to the SLP_TYP and SLP_EN registers.

The following changes are made to Section 9.10.6:

The third sentence of the description for PME_B0_STS is changed to: “If the PME_B0_STS bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN or due to return from AC power failure), then the setting of the PME_B0_STS will generate a wake event, and an SCI (or SMI# if SCI_EN is not set) will be generated.”

The third sentence of the description for PME_STS is changed to: “If the PME_STS bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN or due to return from AC power failure), then the setting of the PME_STS will generate a wake event, and an SCI will be generated.”

The following changes are made to Section 9.10.7:

The second sentence of the description for PME_EN is changed to: “PME can be a wake event from the S1-S4 state or from S5 (if entered via SLP_EN or from AC power recovery, but not power button override).

7. PCIRST# Description Change

In Table 7 of Section 2.5, this sentence in the description for PCIRST# is changed.

“The ICH5 drives PCIRST# inactive a minimum of 1 mS after PWROK is driven active.” is changed to read

“The ICH5 drives PCIRST# inactive a minimum of 1 mS after PWROK and VRMPWRGD are driven active.”

8. APM I/O Decode Correction

The second sentence of Section 9.9 (APM I/O Decode) is being changed to “This register space cannot be moved (fixed I/O location).”

9. SATA PCS Register Changes

Section 11.1.33 (PCS - Port Control and Status Register) is changed as indicated for the following bits:

Bits	Description
1	Port 1 Enabled (P1E) - R/W 0 = Disabled. The port is in the "off" state and cannot detect any devices. 1 = Enabled. The port is in the "on" state and can detect devices.
0	Port 0 Enabled (P0E) - R/W 0 = Disabled. The port is in the "off" state and cannot detect any devices. 1 = Enabled. The port is in the "on" state and can detect devices.

10. Memory Map Table Change

The last row of Table 133 of Section 6.4 (Memory Map) is being replaced as follows:

Memory Range	Target	Dependency/Comments
All other	PCI	Any memory range access that makes it to the ICH5's PCI bus and is not specified in one of the D31:F0 0xE0 - 0xEF registers or below 16MB will be master aborted on PCI.

11. SMBus Host_Busy Bit Correction

Section 14.2.1 HST_STS - Host Status Register is being corrected. Specifically, bit-0 Host_Busy is corrected to read as follows:

0 = Cleared by the ICH5 when the current transaction is completed.

1 = Indicates that the ICH5 is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE or LAST BYTE Registers. The BLOCK DATA BYTE and LAST BYTE registers can be accessed when this bit is set only when the SMB_CMD bits in the Host Control Register are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

12. GEN_CNTL Register Correction

Section 9.1.22, D31:F0;GEN_CNTL has an inaccurate description for System Bus Message Disable (bit-7). It is replaced as follows:

Bit	Description
7	System Bus Message Disable - R/W 1 = Has no effect. (Default) 0 = Disables the ICH5 IOAPIC controller from generating any more system bus interrupt messages. Note: It is possible for the ICH5 to deliver up to 1 system bus interrupt message from the time this configuration bit is set to 0.

13. Assorted Corrections

Section 9.6.3, RTC_REGB has an inaccurate description for the AIE bit. It is replaced as follows:

Bit	Description
5	Alarm Interrupt Enable (AIE) - R/W. This bit is cleared by RTCRST#, but not on any other reset. 0= Disable 1= Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, once an hour, once a day, or once a month.

Table-53 in Section 5.11.5 (Clearing Battery-Backed RTC RAM) is inaccurate and is replaced as follows:

Bit Name	Register Location	Register Location	Bit Location	Default
FREQ_STRAP:[3:0]	BACK_CNTL	D31:F0;D5h	3:0	1111b
AIE	RTC REG B	I/O Space	5	0
AF	RTC REG C	I/O Space	5	0
PWR_FLR	GEN_PMCON_3	D31:F0;A4h	1	0
AFTERG3_EN	GEN_PMCON_3	D31:F0;A4h	0	0
RTC_PWR_STS	GEN_PMCON_3	D31:F0;A4h	2	1
PRBTNOR_STS	PM1_STS	PMBase + 00h	11	0
PME_EN	GPE0_EN	PMBase + 2Ch	11	0
RI_EN	GPE0_EN	PMBase + 2Ch	8	0
NEW_CENTURY_STS	TCO1_STS	TCOBase + 04h	7	0
INTRD_DET	TCO2_STS	TCOBase + 06h	0	0
TOP_SWAP	BACK_CNTL	D31:F0;D5h	5	0
RTC_EN	PM1_EN	PMBase + 02h	10	0

Section 9.10.9, SMI_STS has an inaccurate attribute for the TCO_STS bit (bit-13). It is incorrectly listed as RO. It is actually R/WC.

14. GPIO SMI/SCI Mapping

The notes associated with selected rows of Table 74 (GPIO Implementation) are corrected as follows. Other rows remain unchanged.

GPIO	Type	Alternate Function (Note 1)	Power Well	Tolerant	Notes
GPI0	Input Only	REQA#	Core	5.0 V	<ul style="list-style-type: none"> GPIO_USE_SEL bit 0 enables REQ/GNTA# pair. Input active status read from GPE0_STS bit 16. Input active high/low set through GPI_INV bit 0.
GPI1	Input Only	REQB# or REQ55#	Core	5.0 V	<ul style="list-style-type: none"> GPIO_USE_SEL bit 1 enables REQ/GNTB# pair (see Note 4). Input active status read from GPE0_STS bit 17. Input active high/low set through GPI_INV bit 1.
GPI:[5:2]	Input Only	PIRQ:[E:H]#	Core	5.0 V	<ul style="list-style-type: none"> GPIO_USE_SEL bits {2:5} enable PIRQ:[E:H]#. Input active status read from GPE0_STS bits [18:21]. Input active high/low set through GPI_INV bits [2:5].
GPI6	Input Only	N/A	Core	5.0 V	<ul style="list-style-type: none"> Input active status read from GPE0_STS bit 22. Input active high/low set through GPI_INV bit 6.
GPI7	Input Only	Unmuxed	Core	5.0 V	<ul style="list-style-type: none"> Input active status read from GPE0_STS bit 23. Input active high/low set through GPI_INV bit 7.
GPI8	Input Only	Unmuxed	Resume	3.3 V	<ul style="list-style-type: none"> Input active status read from GPE0_STS bit 24. Input active high/low set through GPI_INV bit 8.
GPI:[10:9]	Input Only	OC:[4:5]#	Resume	5.0 V	<ul style="list-style-type: none"> GPIO_USE_SEL bits [9:10] enable OC:[4:5]#. Input active status read from GPE0_STS bits [25:26]. Input active high/low set through GPI_INV bits [9:10].
GPI11	Input Only	SMBAlert#	Resume	3.3 V	<ul style="list-style-type: none"> GPIO_USE_SEL bit 11 enables SMBAlert#. Input active status read from GPE0_STS bit 27. Input active high/low set through GPI_INV bit 11.
GPI12	Input Only	Unmuxed	Resume	3.3 V	<ul style="list-style-type: none"> Input active status read from GPE0_STS bit 28. Input active high/low set through GPI_INV bit 12.
GPI13	Input Only	Unmuxed	Resume	3.3 V	<ul style="list-style-type: none"> Input active status read from GPE0_STS bit 29. Input active high/low set through GPI_INV bit 13.
GPI:[15:14]	Input Only	OC:[6:7]#	Resume	5.0 V	<ul style="list-style-type: none"> GPIO_USE_SEL bits [14:15] enable OC:[6:7]#. Input active status read from GPE0_STS bits [30:31]. Input active high/low set through GPI_INV bits [14:15].

15. TCO_STS Correction

The TCO_STS bit, bit-13 in D31:F0;SMI_STS, is incorrectly listed as RO in the bit description (Section 9.10.9). This bit is R/WC.

16. SRS/PRS Bit Reference Correction

The SRS and PRS are incorrectly referenced to D31:F0;Offset D0h in fields SEC_SIG_MODE and PRI_SIG_MODE of both IDE_CONFIG registers (D31:F1 and F2 at offset 54h). The correct reference is to D31:F0.

17. GEN2_DEC Correction

The description for Generic I/O Decode Range 2 Base Address (GEN2_BASE) in section 9.1.32, changes to “This address is aligned on a 16-byte boundary and must have address lines 31:16 as 0.”

The note remains unchanged.

18. GPIO_USE_SEL2 Correction

The following note is added to the Description for GPIO_USE_SEL2 (Section 9.12.6):

4. Bit-16 is not implemented because GPIO selection is controlled by bit-8.

19. GP_LVL Default

Table 153 (Registers to Control GPIO Address Map) incorrectly identifies the default value of the GP_LVL register. The correct default value is 1B3F 0000h. This is correctly identified in the register description.

20. IDE MSE Bit

In section 10.1.3 (PCI Command Register) the description for bit-1 is incorrect and is changed to the following:

Bit	Description
1	Memory Space Enable (MSE) - RO

21. USB Port Number Documentation Corrections

In section 5.20.10.1.3, the description of bits 20:23 of the EHCI Host Controller Structural Parameters register indicates an incorrect value for these bits. The sentence is changed to:

“This 4-bit field represents the numeric value assigned to the debug port (i.e., 0001 = port 0).”

The PWAKE_CAP.Port Wake Up Capability Mask (section 13.1.25) bit description is changed to the following:

Bit	Description
8:1	Port Wake Up Capability Mask — R/W. Bit positions 1 through 8 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 0, bit position 2 corresponds to port 1, etc.