



# Intel<sup>®</sup> 82801CA I/O Controller Hub3 (ICH3-S)

Specification Update

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*September 2006*

**Notice:** The Intel<sup>®</sup> I/O Controller Hub 3 (ICH3-S) product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 290739-014



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The Intel® I/O Controller Hub 3 (ICH3-S) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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# Revision History

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Revision	Version	Description	Date
-001	1.0	Initial Release.	February 25, 2002
-002	1.0	Added Errata #18	May 2002
-003	1.0	Added: Errata #19, Updated Errata #15 Specification Clarification #1, #2 Document Change #2, #3, #4	June 2002
-004	1.0	Added: Specification Clarification #3, #4, #5 #6 Document Change #5	July 2002
-005	1.0	Added: Document Change #6	August 2002
-006	1.0	Added: Errata #20 Specification Clarification #7 Document Change #7	September 2002
-007	1.0	Added: Document Change #8	October 2002
-008	1.0	Added: Specification Clarification #8	December 2002
-009	1.0	Added: Additional Identification Markings Added: Specification Change #1	March 2003
-010	1.0	Added: Errata #21 Added: Document Chage #9	May 2003
-011	1.0	Added: Document Change #10	June 2003
-012	1.0	Added: Errata #22 Added: Specification Clarification #9, 10	July 2003
-013	1.0	Added: Errata #23, 24	January 2004
-014	1.0	Added: Errata #25	September 2006



## Preface

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This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

### Affected Documents/Related Documents

Title	Order
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	290733-001

**Note:** Throughout the Intel® ICH3-S Specification Update, all references to ICH3 refer to the Intel® ICH3-S part unless specifically noted otherwise.

### Nomenclature

**Errata** are design defects or errors. Errata may cause the ICH3-S's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

# Summary Table of Changes

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The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® 82801CA I/O Controller Hub 3 (ICH3-S). Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or

(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

### Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum is intended to be fixed in a future stepping of the component.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

## Errata (Sheet 1 of 2)

No.	B1 Stepping	Status	ERRATA
1	X	No Fix	I/O APIC and C2/C3
2	X	No Fix	AC'97 "Missed Sample"
3	X	No Fix	Power-button/CF9 Reset
4	X	No Fix	Special Cycle Non-Zero Address
5	X	No Fix	LPC Reset Timing Issue
6	X	No Fix	USB Impedance Compensation Issue
7	X	No Fix	AC'97 Link Reset Race Condition
8	X	No Fix	SMBus Arbitration Erratum
9	X	No Fix	I <sup>2</sup> C Read Command issue
10	X	No Fix	PERR# Response Issue
11	X	No Fix	PERR# Detection Issue
12	X	No Fix	SE0 During Resume Causes Disconnect

## Errata (Sheet 2 of 2)

No.	B1 Stepping	Status	ERRATA
13	X	No Fix	ATA Rising Edge Slew Rate Issue
14	X	No Fix	Master Abort Mode issue
15	X	No Fix	IDE Hang Issue
16	X	No Fix	SMBus NACK and Proc_Call Issue
17	X	No Fix	Delayed Transaction Timeout Bit
18	X	No Fix	2DW I/O Cycle Native IDE Issue
19	X	No Fix	AC '97 Overrun FIFO Error Bit Not Set
20	X	No Fix	RTC I/O Read
21	X	No Fix	PCI Non-Linear Addressing
22	X	No Fix	IDE MW DMA Mode-1 Tdh
23	X	No Fix	USB Buffer Overrun
24	X	No Fix	LPC Starvation
25	X	No Fix	Full-speed USB ISOC End of Packet

## Specification Changes

No.	SPECIFICATION CHANGES
1	Delayed Transaction Discard Timer

## Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	RTC Set Bit
2	12-Clock Retry Enable
3	LPC LPCPD# Protocol Clarification
4	USB Legacy Keyboard Mouse Control
5	RTC Voltage
6	XOR Chain#4 Output and Chain List Clarification
7	Native Mode IDE/ACPI S3 Resume Hang Avoidance
8	PCI Bus Interface
9	Memory Decode Range Table
10	PERR# Implementation
11	SCI Creation During Non-ACPI Operation
12	LPC Cycle Clarification

## Documentation Changes

No.	DOCUMENTATION CHANGES
1	PCI Device Revision ID Table
2	SUSCLK AC Timing Parameters
3	GPIO[22] & GPIO[24] Logical States
4	TCO Registers
5	USB PORTSC Register
6	Speed Strapping
7	Operating Range for CPU Voltage: CPU I/F
8	GPIO[18,19,20,22,23,24] Mapping
9	Figure 2-2 (RTC Circuit) Correction
10	Wake Events from an AC Power Failure

# Identification Information

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## Markings

ICH3-S Stepping	S-Spec	Top Marking	Notes
B1	SL632	FW82801CA	Production

# Errata

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## 1. I/O APIC and C2/C3

**Problem:** Interrupts get missed when C-states and I/O APIC are enabled.

**Implication:** System clock is observed running slower when C2/C3 and I/O APIC are enabled and IRQ8 is used for system clock update. Result - time lost. This phenomenon is due to a race condition that exists between C2/C3 break events and the latency of interrupt messages on APIC bus.

**Workaround:** C2/C3/C4 and IOAPIC cannot be used together. De-feature I/O APIC if using C2/C3/C4.

Note: See Platform Design Guide on recommended implementation of serial I/O APIC bus.

**Status:** There are no plans to fix this erratum.

## 2. AC '97 "Missed Sample"

**Problem:** If an incoming data overrun occurs on AC-link within a 2 clock time window of an AC '97 write completion on the hub interface, the AC '97 controller will not see the FIFOE status bit.

**Implication:** There is a possibility of missing a single sample of incoming (Modem In, Mic In, or PCM In) AC '97 data. For audio data, this will be undetectable. For modem, sample overrun could cause a single bit corruption. On these rare instances, SW will request a packet re-transmit as result of CRC error detection, resulting in a negligible performance hit (modem data packet re-tries occur frequently due to telephone line noise). Neither Audio nor Modem drivers are affected, since they do not implement overrun error handlers. The boundary conditions required for this to occur are extremely unlikely. This issue has only been observed in artificial, highly stressed system test environments.

**Workaround:** Not required.

**Status:** There are no plans to fix this erratum.

## 3. Power-button/CF9 Reset

**Problem:** If the power-button is pressed (PWRBTN# is asserted) during a CF9 hard reset event (an I/O write of 06h to CF9h), or if a CF9 hard reset sequence is initiated while the power-button is depressed, the ICH3 will behave as if a power-button override event has occurred and transition the system to S5 state (off).

**Implication:** The system may unexpectedly transition to the S5 state (turn off). The user will have to awaken the system by pressing the power-button.

**Workaround:** Software must test the PWRBTN# status bit before attempting a CF9 hard reset; this sequence can reduce the boundary of this issue.

**Status:** There are no plans to fix this erratum.

#### 4. Special Cycle Non-Zero Address

**Problem:** Special Cycles immediately followed by any cycle(s) (within 3 hub interface clocks) may result in the ICH3 driving non-zero data during the address phase of the special cycle. The PCI specification only requires that stable data be driven during the address phase; it does not require that address bits 31:0 be all zeros.

**Implication:** Non-PCI compliant devices may attempt to claim this special cycle and the device may not function properly. This has only been seen on one PCI graphics card that is no longer produced.

**Workaround:** None.

**Status:** There are no plans to fix this erratum.

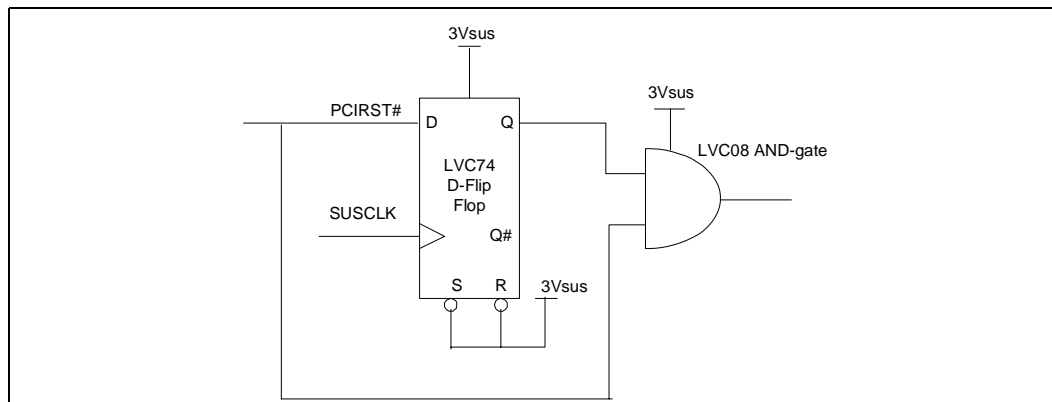
#### 5. LPC Reset Timing Issue

**Problem:** The ICH3 specified 1–3 RTC timing of SUS\_STAT# inactive to PCIRST# inactive violates the LPC specification of “at least 60  $\mu$ s.”

**Implication:** Some LPC devices may not properly reset resulting in failure of the system to boot or resume from a sleep state.

**Workaround:** Use any one of these three workarounds:

1. Delay PCIRST# by 1 SUSCLK using a D-flop and an AND gate to the LPC devices.



2. Do a CF9 hard reset within the first 100 ms of POST.
3. Do not connect the SUS\_STAT# to the SIO PD input; instead, implement an external pull-up resistor on the PD input of the SIO.

**Status:** There are no plans to fix this erratum.

#### 6. USB Impedance Compensation Issue

**Problem:** A setup timing issue exists in the ICH3's impedance compensation circuit which can cause the USB buffers to shut off, leading to missed USB transmit packets.

**Implication:** This is likely to result in data loss or may cause data corruption.

**Workaround:** A BIOS workaround has been validated.

Contact your local Intel field representative if you require more BIOS information.

**Status:** There are no plans to fix this erratum.

## 7. AC-Link Reset Race Condition

**Problem:** If an AC '97 reset is initiated (via GLB\_CNT:[1]) just as a new frame is starting a race condition between AC\_RST# asserting and AC\_SDIN transitioning from “Ready=1” to ground, due to the reset, may cause an unexpected wake event (SMI) if AC '97 wake events are enabled (via GPE0\_EN).

**Implication:** This will result in an unexpected wake event (SMI) that may not be comprehended by the SMI handler resulting in repeated SMIs.

**Workaround:** Early in enumeration disable AC '97 wake event and re-enable it after enumeration. BIOS must disable SMI and PME generation when doing a reset to or powering down the codecs. BIOS should clear the related status registers and then re-enable SMI and PME generation.

**Status:** There are no plans to fix this erratum.

## 8. SMBus Arbitration Erratum

**Problem:** ICH3 will not detect a bus collision when attempting to STOP at the end of a SMBus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, ICH3 does not set the Bus Error bit.

**Implication:** A master attempting a transfer that had actually “lost” may think that its transaction was completed when it was not completed.

**Workaround:** None.

**Status:** There are no plans to fix this erratum.

## 9. I<sup>2</sup>C Read Command Issue

**Problem:** ICH3 uses HST\_D0 register (D31:F3, offset 05h) as the byte count register instead of depending on the LAST\_BYTE bit in Host Control register (D31:F3, offset 02h: bit5) to end the transaction.

**Implication:** The transaction will stop pre-maturely if HST\_D0 contains a number smaller than the intended transaction. De-feature I<sup>2</sup>C read command.

**Workaround:** No workaround for 10-bit addressing I<sup>2</sup>C devices. The SMBus read command for 7-bit addressing may be used with I<sup>2</sup>C devices.

**Status:** There are no plans to fix this erratum. Defeature the I<sup>2</sup>C Read command.

## 10. PERR# Response Issue

**Problem:** If ICH3's Parity Error Response Enable (PER) Bit in Bridge\_CNT Register (D30:F0, offset 3Eh: bit 0) is disabled (default), it will block PERR# from being asserted when a data Parity Error is detected on the PCI bus during LPC or legacy DMA master read cycles, or when the ICH3 is the target for write cycles to Device 31 Function 0 and Function 3. This bit should only block PERR# from being asserted when a PCI data Parity Error is detected during PCI-to-memory writes or CPU-to-PCI read cycles.

This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

**Implication:** PERR# will not be asserted when the PCI Parity Error is detected during LPC or legacy DMA master read cycles, or when ICH3 is the target for write cycles to Device 31 Function 0 and Function 3.

**Workaround:** BIOS needs to set PER of Bridge\_CNT when the parity error detection is supported on LPC or legacy DMA.

**Status:** There are no plans to fix this erratum.

## 11. PERR# Detection Issue

**Problem:** ICH3's Detected Parity Error (DPE) Bit in SECSTS Register (D30:F0, offset 1Eh: bit 15) and PCISTA Register (D31:F0, offset 06h: bit 15) will get set when PERR# is asserted by external PCI devices.

This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

**Implication:** DPE bit of SECSTS and PCISTA may get erroneously set. These bits are used to report status only. No interrupts will be occurred.

**Workaround:** BIOS needs to check DPE bit on all external PCI devices, if PERR# was been asserted by the external PCI devices, BIOS needs to clear DPE of SECSTS and PCISTA because these bits may get erroneously set.

**Status:** There are no plans to fix this erratum.

## 12. SE0 During Resume Causes Disconnect

**Problem:** A transient SE0 during an upstream resume signal from the USB peripheral to the ICH3 while the system is in S3/S4 sleep states will cause the ICH3 to register a disconnect. This violates the USB Rev 1.1 specification.

**Implication:** The implication is Operating System dependent. It can range from additional latency on a resume before the USB device is functional (after a resume), to the USB device no longer works after a resume - in which case a system reboot must be done to obtain USB device functionality. In all cases the rest of the system does resume.

**Workaround:** None

**Status:** There are no plans to fix this erratum.

## 13. ATA Rising Edge Slew Rate Issue

**Problem:** ICH3's ATA Rising edge slew rate ( $S_{RISE2}$ ) for DD[15:0] does not meet Ultra ATA/100 Specification.

**Implication:** Although ICH3 does not meet  $S_{RISE2}$ , ICH3 does meet the ATA signal integrity guidelines and AC timings. Furthermore, no failures have been reported in system validation or customers to date as a result of this erratum.

**Workaround:** None.

**Status:** There are no plans to fix this erratum.

## 14. Master Abort Mode Issue

**Problem:** ICH3 Master Abort Mode (BRIDGE\_CNT – Bridge Control Register, D30:F0, offset 3E–3Fh, bit 5) is a new function. It was implemented incorrectly. A missing qualification can cause a Target Abort signal to a PCI agent that was uninvolved in the transfer.

**Implication:** ICH3 could Target Abort the wrong bus master.

**Workaround:** De-feature Master Abort Mode. Power on default is Master Abort Mode bit is disabled. BIOS needs to make sure this bit is not enabled.

**Status:** There are no plans to fix this erratum.

## 15. IDE Hang Issue

**Problem:** An arbitration deadlock in the ICH3 may occur if IDE traffic is combined with heavy graphic traffic and internal/external PCI Bus Master traffic to memory.

**Implication:** This issue may lockup the IDE bus master causing a system hang. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

**Workaround:** BIOS needs to set configuration register (Device 31, Function +0, offset FCh, bit 23) to prevent the arbitration deadlock. Contact your local Intel field representative if you require more BIOS information.

**Status:** There are no plans to fix this erratum.

## 16. SMBus NACK and Proc\_Call Issue

**Problem:** ICH3-S SMBus controller fails to respond after being NACKed on the 4th data phase when using the SMBus command Process Call (with or without with I<sup>2</sup>C enabled).

**Implication:** This issue may lockup the SMBus controller and cause system to stop responding. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by known commercial applications.

**Workaround:** No Workaround.

**Status:** There are no plans to fix this erratum.

## 17. Delayed Transaction Timeout Bit

**Problem:** After a delayed transaction has been serviced the discard timer is not reset, which incorrectly times out. This timeout sets the SERR# Due to Delayed Transaction Timeout bit (D30:F0:92h:Bit 1). This may result in generation of SERR# based NMIs if the SERR# enable on Delayed Transaction Timeout bit (D30:F0:90h:Bit 1) is set to a '1' by software or system BIOS.

**Implication:** This erratum may cause excessive NMIs to occur which impacts system performance.

**Workaround:** A BIOS workaround has been identified. See ICH3 BIOS Spec and Updates.

**Status:** There are no plans to fix this erratum.

## 18. 2DW I/O Cycle Native IDE Issue

**Problem:** An I/O read crossing a DWORD boundary being sent from CPU to the ICH3-S may not complete correctly. The ICH3-S will treat such a transaction as two single-DW I/O accesses. If native-IDE addressing is enabled, the ICH3-S will return the first I/O cycle completion request to the MCH, but the second I/O cycle may get decoded to the IDE controller instead of its intended address.

**Implication:** System may hang while CPU waits for return of I/O cycle.

**Workaround:** Disable Native Mode IDE. See ICH3-S BIOS Spec and Updates for details on BIOS workaround.

**Status:** There are no plans to fix this erratum.

## 19. AC '97 Overrun FIFO Error Bit Not Set

**Problem:** The ICH3-S may set the FIFOE Bit in the Input Status Register after a software overrun error occurs on a highly stressed system. The ICH3-S should only set the FIFOE bit on a hardware overrun. Bit affected depends on which stream is currently overrun:

PCM IN - PISR (D31:F5:I/O Offset NABMBAR + 06h:Bit 4)

Microphone IN - MCSR (D31:F5:I/O Offset NABMBAR + 26h:Bit 4)

Modem IN - MISR (D31:F6:I/O Offset NABMBAR + 06h:Bit 4)

**Implication:** Driver vendors typically do not use this status bit in their production drivers.

**Workaround:** None

**Status:** There are no plans to fix this erratum

## 20. RTC I/O Read

**Problem:** Under certain conditions, a CPU generated I/O read to RTC (Real Time Clock) registers 0-9 may return an incorrect value. The issue occurs on the read path from the RTC registers and the RTC value in the registers is not impacted. Should the certain conditions occur, one or more of the bits read from the RTC registers may be incorrect. The issue has only been found using a synthetic test environment and has not been seen using commercially available software.

**Implication:** An operating system or software applications which synchronizes the time/date value with the RTC registers may get an incorrect value.

**Workaround:** BIOS workaround is available in the *Intel® ICH3-S BIOS Specification Update Rev 2.01*. The workaround does take into account multiple CPU's and Hyper Threading. The workaround uses timers to zero-in on the window where invalide RTC I/O read data could be returned. Using the software SMI, HPET timers and port 71 traps, the BIOS will ensure that there are no accesses to the RTC during this timing window.

**Status:** No fix.

## 21. PCI Non-Linear Addressing

**Problem:** If a PCI Memory Read Multiple or Memory Read Line transaction falls at the last DW of a 32B cache line boundary and non-linear addressing (cache-line wrap mode) is used the ICH3-S will pre-fetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent CPU cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

**Implication:** System hang only seen in synthetic test environment. No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line

**Workaround:** None.

**Status:** No fix.

## 22. IDE MW DMA Mode-1 Tdh

**Problem:** Data hold time of MW DMA mode-1 writes may not meet ATA specifacaiton.

**Implication:** None known.

**Workaround:** Program the controller to PIO Mode-4 instead.

**Status:** No fix.

**23. USB Buffer Overrun**

**Problem:** If a USB full-speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20  $\mu$ S of system latency) and the USB FIFO begins to empty during a 30 nS window immediately prior to the overrun event actually occurring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

**Implication:** Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behavior. There is no known exposure with real world applications.

**Workaround:** None.

**Status:** No Fix.

**24. LPC Starvation**

**Problem:** Latency issues on LPC may occur if a PCI bus master is performing large upstream burst to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may get delayed until the PCI device completes its transaction and de-asserts its REQ#.

**Implication:** Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

**Workaround:** None.

**Status:** No Fix.

**25. Full-speed USB ISOC End of Packet**

**Problem:** If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

**Implication:** None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

**Workaround:** None.

**Status:** No Fix.

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# Specification Changes

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## 1. Delayed Transaction Discard Timer

Section 8.1.27 describes the ICH3-S Configuration Register. Bit2 is now defined as indicated.

2	<b>Delayed Transaction Discard Timer - R/W</b> When set to 1 this bit shortens all delayed transaction discard timers from 32 uS to 4 uS.  Note: Setting this bit may improve system performance issues with certain non-optimally behaved PCI devices but may violate the PCI-to-PCI Bridge Architecture Specification Rev 1.1 (section 5.3.2).
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# Specification Clarifications

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## 1. RTC SET Bit Clarification

The SET bit (bit-7) in RTC\_REGB should be set then cleared early in BIOS POST after each power up directly after inserting the coin-cell battery into the mainboard.

## 2. 12-Clock Retry Enable

The description for the 12 Clock Retry Enable bit (bit-1) in the Device 30 F0; CNF (50h) register (Section 8.1.27) is incorrect. There is no relationship to PCI locked cycles. Change to:

12 Clock Retry Enable - R/W, System BIOS must set this bit for the PCI compliance.

1 = The ICH3-S will retry a PCI to memory cycle (reads or write) if the ICH3-S is not able to complete the transfer in 12 PCI clocks.

0 = The ICH3-S will insert as many wait states as needed to complete the PCI to memory cycle.

## 3. LPC LPCPD# Protocol Clarification

The LPC specification defines the LPCPD# protocol where there is at least 30uS from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states which does not include asynchronous reset events. The ICH3-S will assert both SUS\_STAT# (connects to LPCPD#) and PCIRST# (connects to LRST#) at the same time when the core logic is reset (via CF9h, PWOK or SYS\_RESET#, etc). This is not inconsistent with the LPC LPCPD protocol.

## 4. USB Legacy Keyboard Mouse Control

- In Section 11.1.16 (USB\_LEGKEY) add the following note to bits [15, 11:8, 6]:

**Note:** This bit reports same value in all USB UHCI controllers.

- In Section 11.1.16 (USB\_LEGKEY) and the following note to bits [7, 5, 3:0]:

**Note:** Setting this bit in any controller enables the function.

## 5. RTC Voltage

- In table 16-6 (Other DC Char) replace VccRTC with the following:

VccRTC	Powered by Coin Cell Battery	2.0	3.3	V
	Powered by Power Supply	2.0	3.6	V

## 6. XOR Chain #4 Output and Chain List Clarification

Table 18-3 XOR Chain #4 is made up of two independent XOR chains with two independent outputs. The first chain starts at SDD8 and ends with the output GPIO8. The second chain starts at PME# and ends with the output BATLOW#. Replace Table 18-6 with corrected table sequence below:

**Table 18-3. XOR Chain #4 (RTCRST# Asserted for 7 PCI Clocks While PWROK Active)**

Pin Name	Ball #	Notes	Pin Name	Ball #	Notes
SDD8	W13	Top of 1st XOR Chain	OC0#	E12	Last in the 1st XOR Chain
SDD6	AA13	2nd signal in XOR	<b>GPIO8</b>	<b>W2</b>	<b>1st OUTPUT</b>
SDD5	Y14		PME#	W1	Top of 2nd XOR Chain in XOR #4
SDD7	W15		GPIO25	W3	2nd signal in XOR
SDD10	Y15		PCIRST#	Y1	
SDD11	AC16		GPIO13	Y2	
SDD3	AB16		GPIO28	Y3	
SDD9	Y16		GPIO12	Y4	
SDD12	AB17		SLP_S5#	AA2	
<del>SDD15</del> -SDD2	<del>AC18</del> - AC17		GPIO27	W4	
SDD4	W16		SMLINK1	AB2	
<del>SDIOW#</del> SDD13	<del>AA18</del> AA17		PWRBTN#	AB1	
<del>SDD2</del> -SDD15	<del>AC17</del> AC18		CLKRUN#	AC2	
SDD0	Y17		SMLINK0	AC3	
SDDREQ	AB18		SUSCLK	AA4	
SDD14	Y18		SUS_STAT#	AB4	
<del>SDD13</del> SDIOW#	<del>AA17</del> - AA18		SMBCLK	AC4	
SDD1	W17		SLP_S3#	AA5	
SIORDY	AB19		SMBDATA	AB5	
SDIOR#	AC19		SMBALERT#/GP IO11	AC5	
SDDACK#	Y19		OC4#	A12	
SDA1	AA19		OC3#	B12	
SDA2	AB20		OC2#	C12	
SDA0	AC20		OC1#	D12	
SDCS3#	AC22		OC5#	A11	
SDCS1#	AC21		<del>AC_SDIN0</del>	<del>B11</del>	
HI7	T23		AC_RST#	D11	
HI11	R19		USBP0P	D19	
HI6	R20		USBP0N	D18	

Pin Name	Ball #	Notes
HI5	R22	
HI9	P19	
HI4	P21	
HI_STB	N22	
HI10	N19	
HI3	N20	
HI8	M19	
HI1	M21	
HI2	M23	
HI0	L22	
HICOMP	K19	
APICD0	J20	
APICD1	J21	
FERR#	J22	
SERIRQ	H22	
GPIO38	H21	
SPKR	H23	
GPIO41	G21	
GPIO39	G23	
GPIO40	F23	
GPIO43	E23	
GPIO42	D23	

Pin Name	Ball #	Notes
USBP1P	A19	
USBP1N	A18	
USBP2P	E17	
USBP2N	E16	
USBP3P	B17	
USBP3N	B16	
USBP4P	D15	
USBP4N	D14	
USBP5P	A15	
USBP5N	A14	
LAN_TXD2	A10	
LAN_TXD1	C10	
EE_SHCLK	D10	
LAN_RXD2	A9	
LAN_TXD0	B9	
EE_CS	E9	
LAN_RXD1	A8	
LAN_RXD0	C8	
EE_DIN	D8	
EE_DOUT	E8	
LAN_RSTSYNC	D7	Last in the 2nd XOR Chain
<b>BATLOW#</b>	<b>AB3</b>	<b>2nd OUTPUT</b>

## 7. Native IDE/ACPI S3 Resume Hang Avoidance

System BIOS must clear the Interrupt bit (bit 2) in Bus Master IDE Status Register for both primary and secondary channels prior to passing control to the OS during resume from S3 state (STR). This ensures that the pending IDE interrupt(s) are cleared when the control is passed to the OS. The registers are located in I/O space via BM\_BASE register (Bus 0: Device 31: Function 1: Register 20-23h) at offset 02h and offset 0Ah, respectively. Failure to do this may result in system hang when the OS starts executing resume sequence from S3 (STR) under certain conditions.

These conditions include a combination of the following:

- Only a single channel of IDE is enabled (either Primary or Secondary)
- Native IDE Mode capability is reported by the BIOS
- OS is capable of dynamically switching from Legacy IDE Mode to Native IDE Mode

A system hang may occur if there exists a pending IDE Interrupt status bit during the legacy IDE Mode to Native IDE mode sequence, the OS may not clear the IDE interrupt(s), resulting in an apparent hang condition (interrupt storm).

### 8. PCI Bus Interface

Add Note to 5.1.1 (PCI Bus Interface)

Note: PCI Bus Masters should not use memory ~~PAM~~ area locations as a target if that ~~PAM~~ area is programmed to be anything but Read/Write.

### 9. Memory Decode Range Table

In Table 6-5, add the following comment under Dependency/Comments:

Memory Range	Target	Dependency/Comments
All other	PCI	None. If the address is below 16M, is not in one of the above BIOS Ranges, and positive decode is disabled; then the cycle will be forwarded to LPC as a standard LPC memory cycle. If the address is above 16M, if the cycle is not claimed by a device on PCI and not the Intel ICH3, then the cycle will Master-Abort on PCI.

### 10. PERR# Implementation

The ICH3-S does not escalate a data parity mismatch reported by a PCI device (PERR#) across the P2P bridge. The PCI Specification or P2P bridge spec does not require PERR# escalation across P2P bridge.

For certain applications, it may be desirable to generate an SMI or NMI upon PERR# assertion by a PCI device. The device/driver is expected to handle such situations by retrying the transactions or escalating to the OS via device driver. Alternatively, external circuitry can be added to platforms to drive SMI or NMI upon PERR# assertion.

### 11. SCI Creation During Non-ACPI Operation

Adding register bit definition to Section 9.8.1.5 (GPI Routing Control Register) of the Datasheet: Software must set this bit field to generate the appropriate type of system interrupt, depending on how the SCI\_EN bit is set. For example, if the SCI\_EN bit is set, then this field must be programmed to 00b or 10b. If the SCI\_EN bit is cleared, then this field must be programmed to 00b or 01b. Software must also update this field if the SCI\_EN bit is changed.

## 12. **LPC Cycle Clarification**

The following changes are made to Table 5-2 LPC Cycle Types Supported in section 5.3.1.1:

- “See Note 1” is removed from the comment column for both I/O Read and I/O Write cycle types.
- “See Note 1” is added to the comment column for both Memory Read and Memory Write cycle types.

# Documentation Changes

## 1. PCI Device Revision ID Table

PCI Revision ID Register values (PCI offset 08h) for all ICH3-S functions are listed in the following table.

This information is not listed in the datasheet. This is the standard reference document for all Revision ID values.

Device, Function	Description	Intel® ICH3-S B1 Rev ID
D8, F0	LAN	42h
D29, F0	USB Controller 1	02h
D29, F1	USB Controller 2	02h
D29, F2	USB Controller 3	02h
D30, F0	P2P Bridge	42h
D31, F0	P2L Bridge	02h
D31, F1	IDE	02h
D31, F3	SMBus	02h
D31, F5	AC '97 Audio	02h
D31, F6	AC '97 Modem	02h

### NOTES:

1. From a software perspective, the integrated LAN Controller (D8:F0) appears to reside on the secondary side of the ICH3-S virtual PCI-to-PCI Bridge. This is typically Bus 1, but may be assigned a different number, depending upon system configuration.
2. The ICH3-S integrated LAN Controller (D8:F0) provides support for configurable Subsystem ID and Subsystem Vendor ID fields. After reset, the LAN Controller automatically reads addresses Ah through Ch of the EEPROM. The LAN Controller checks bits 15:13 in the EEPROM word Ah.

## 2. SUSCLK AC Timing Parameters

The AC timing parameters for SUSCLK are not present in the datasheet. The following section has now been added to Table 16-7. Clock Timings:

Sym	Parameter	Min	Max	Unit	Notes	Figure
	Suspend Clock (SUSCLK)					
$f_{\text{susclk}}$	Operating Frequency	32		KHz	6	
t14	High Time	10		us	6	16-1
t15	Low Time	10		us	6	16-1

### 3. GPIO[22] & GPIO[24] Logical States

#### GPIO[22] Logical State During/After PCIRST#

In Table 3-4 Power Planes and States for Output and I/O Signal of the datasheet, the definitions for the logical state of GPIO[22] during and immediately after PCIRST# are incorrect. The table should read as follows:

Signal	Power Plane	During PCIRST# <sup>4</sup> / RSMRST# <sup>5</sup>	Immediately after PCIRST# <sup>4</sup> / RSMRST# <sup>5</sup>	S1	S3	S4/S5
GPIO[22]	Resume I/O	Low	Low	Defined	Defined	Defined

#### GPIO[24] Logical State During/After RSMRST#

In Table 3-4 Power Planes and States for Output and I/O Signal of the datasheet, the definitions for the logical state of GPIO[24] during and immediately after RSMRST# are incorrect. The table should read as follows:

Signal	Power Plane	During PCIRST# <sup>4</sup> / RSMRST# <sup>5</sup>	Immediately after PCIRST# <sup>4</sup> / RSMRST# <sup>5</sup>	S1	S3	S4/S5
GPIO[24]	Resume I/O	High	High	Defined	Defined	Defined

### 4. TCO Registers

TCOBase IO locations are incorrect for the following registers:

- Section 9.9.2: TCOBase+0 is TCO\_RLD (not TCO1\_RLD) and the default value is 00h (not 0000h)
- Section 9.9.3: TCOBase+1 is TCO\_TMR (not TCO1\_TMR) and the default value is 04h (not 0004h). Description incorrectly states “Value of 0-3h will be ignored..” where actually values of 0-1h will be ignored
- Section 9.9.4: TCOBase+2 is TCO\_DAT\_IN (not TCO1\_DAT\_IN) and the default is 00h (not 0000h). The description also incorrectly refers to “OS TCO\_SMI” and “TCO\_STS” which should be “SW\_TCO\_SMI” and “TCO1\_STS”
- Section 9.9.5: TCOBase+3 is TCO\_DAT\_OUT (not TCO1\_DAT\_OUT) and the default value is 00h (not 0000h)

### 5. USB PORTSC Register

In Section 11.2.7 bit 9 Port Reset is R/W not R/O.

## 6. Speed Strapping

In Section 5.11.3, Table 5-33, remove the sentence:

State Exiting	ICH3
S1	There is no processor reset, so no frequency strap logic is used.
S3, S4, S5, or G3	Based on PWROK going active, the ICH3 will deassert PCIRST#, and based on the value of the FREQ_STRAP field (D31:F0, Offset D4), the ICH3 will drive the intended core frequency values on A20M#, IGNNE#, NMI, and INTR. <del>The ICH3 will hold these signals for 120 ns after CPU_RST# is deasserted by the Host controller.</del>

## 7. Operating Range for CPU Voltage: CPU I/F

In Section 3.1, Table 3-1, change the CPU I/F voltage range:

CPU I/F (.95 - 2.625V) ~~(1.3 -- 2.5V)~~

## 8. GPIO[18,19,20,22,23,24] Mapping

In Section 5.14.1, Table 5-51 GPIO Mapping, add to the table:

Name	Usage	Muxed	I/O	Pwr Plan	Tolerant	Wake event support	Wake from State	After RSMRST #	After PCIRST#
GPIO[18]		No	O	Core	5.0V	---	---	High	Blink <sup>1</sup>
GPIO[19]		No	O	Core	5.0V	---	---	High	High
GPIO[20]		No	O	Core	5.0V	---	---	High	High
GPIO[22]		No	OD	Core	5.0V	---	---	High-Z	High-Z
GPIO[23]		No	O	Core	5.0V	---	---	Low	Low
GPIO[24]		No	I/O	Resume	3.3V	---	---	High	High

## 9. Figure 2-2 (RTC Circuit) Correction

The following note is added to the list of notes inside Figure 2-2 to be consistent with requirements:

Note - Diodes are schottky.

## 10. Wake Event from an AC Power Failure

### 1) Make the following changes to Section 5.12.7.2 Table 5-41

**Table 5-41 Causes of Wake Events**

Cause	States Can Wake From	How Enabled
RTC Alarm	S1–S5 (Note 1)	Set RTC_EN bit in PM1_EN Register
Power Button	S1–S5	Always enabled as Wake event
GPI[0:n]	S1–S5 (Note 1, 3)	GPE1_EN Register
USB	S1–S4	Set USB1_EN, USB 2_EN or USB3_EN bits in GPE0_EN Register
LAN	S1–S5	Will use PME#. Wake enable set with LAN logic.
RI#	S1–S5 (Note 1)	Set RI_EN bit in GPE0_EN Register
AC '97	S1–S5	Set AC97_EN bit in GPE0_EN Register
Primary PME#	S1–S5	PME_B0_EN bit in GPE0_EN Register
Secondary PME#	S1–S5 (Note 1)	Set PME_EN bit in GPE0_EN Register.
SMBALERT#	S1–S4	SMB_WAK_EN in the GPE0 Register
SMBus Slave Message	S1–S5	Wake/SMI# command always enabled as a Wake Event. <b>Note:</b> SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override.
SMBus Host Notify Message Received	S1–S5	HOST_NOTIFY_WKEN bit SMBus Slave Command Register. Reported in the SMB_WAK_STS bit in the GPE0_STS Register.

**NOTES:**

1. This will be a wake event from S5 only if the sleep state was entered by setting the SLP\_EN and SLP\_TYP bits via software **or from powerfailure**.
2. If in the S5 state due to a powerbutton override, the possible wake events are due to Power Button, Hard Reset Without Cycling (See Command Type 3 in Table 5-93), and Hard Reset System (See Command Type 4 in Table 5-93).
3. This is a wake event from S5 only if the sleep state was entered by setting the SLP\_EN and SLP\_TYP bits via software.

### 2) Make the following changes to Section 5.12.3

#### 5.12.7.3 Sx–G3–Sx, Handling Power Failures

In server systems, power failures can occur if the AC power is cut (a real power failure) or if the system is unplugged. In either case, PWROK and RSMRST# are assumed to go low.

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER\_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system will remain in an S5 state (unless previously in S4). There are ~~only three~~ **four** possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN\_STS bit is reset. When the ICH3 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because Vcc-standby goes high before RSMRST# goes high) and the PWRBTN\_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI\_STS bit will be set and the system will interpret that as a wake event.
3. **RTC Alarm:** The RTC\_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN\_STS the RTC\_STS bit is cleared when RSMRST# goes low.
4. **PME:** PME\_STS or PME\_B0\_STS, if enabled, will wake the system from S5 if S5 is entered from an AC power failure or if entered by a write to SLP\_TYP and SLP\_EN registers.

The ICH3 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK\_FLR bit is set. If RSMRST# goes low, PWR\_FLR is set.

**Note:** Although PME\_EN is in the RTC well, this signal cannot wake the system after a power loss. PME\_EN is cleared by RTCRST#, and PME\_STS is cleared by RSMRST#.

### 3) Make the following changes to Section 9.8.3.7

13	<p><b>PME_B0_STS</b>—R/W.</p> <p>0 = The default for this bit is 0. Writing a 1 to this bit clears this bit.</p> <p>1 = Set to 1 by the ICH3 when any internal device on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit is set and the system is in an S0 state, the setting of the PME_B0_STS bit generates an SCI (or SMI# if SCI_EN is not set). If the PME_B0_STS bit is set and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN or <b>due to return from AC power failure</b>), the setting of the PME_B0_STS bit generates a wake event, and an SCI (or SMI# if SCI_EN is not set) is generated. If the system is in an S5 state due to power button override, the PME_B0_STS bit does not cause a wake event or SCI.</p>
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### 4) Make the following changes to Section 9.8.3.8

13	<p><b>PME_B0_EN</b>—R/W. Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. PME_B0_STS can be a wake event from the S1–S4 states, or from S5 (if entered via SLP_TYP and SLP_EN or <b>AC power failure</b>), but not Power Button Override. This bit defaults to 0. It is only cleared by Software or RTCRST#. It is not cleared by CF9h writes.</p>
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11	<p><b>PME_EN</b>—R/W.</p> <p>0 = Disable.</p> <p>1 = Enables the setting of the PME_STS to generate a wake event and/or an SCI. PME# can be a wake event from the S1–S4 state or from S5 (if entered via <b>SLP_TYP</b> and SLP_EN or <b>AC power failure</b>, but not power button override).</p>
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