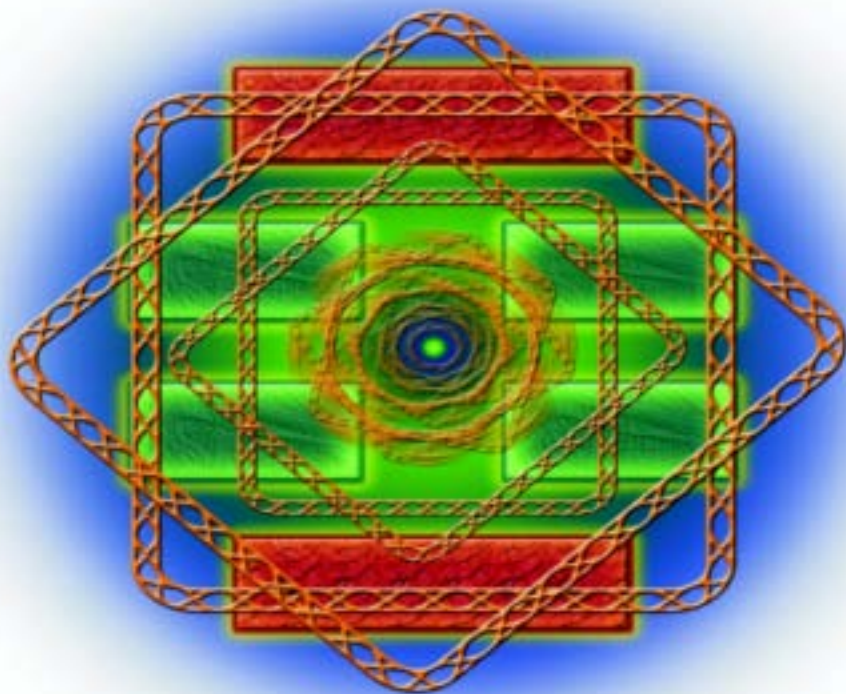


Mastering High Performance Multiprocessor Signaling

Electrical design with the Intel® QuickPath Interconnect

By Dave Coleman and Michael Mirmak



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