



DOUBLE DATA RATE (DDR) SDRAM

MT46V32M8 – 8 MEG X 8 X 4 BANKS
MT46V16M16 – 4 MEG X 16 X 4 BANKS

For the latest data sheet revisions, please refer to the
 Micron Website: www.micron.com/dramds

Features

- 200 MHz Clock, 400 Mb/s/p data rate
- Low Latency DDR400B (3-3-3)
- $V_{DD} = +2.60V \pm 0.10V$
- $V_{DDQ} = +2.60V \pm 0.10V$
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- t_{RAS} lockout ($t_{RAP} = t_{RCD}$)

OPTIONS

- Configuration
 - 32 Meg x 8 (8 Meg x 8 x 4 banks)
 - 16 Meg x 16 (4 Meg x 16 x 4 banks)
- Plastic Package
 - 66-Pin TSOP (400mil with 0.65mm pin pitch)
 - 66-Pin TSOP Lead-free (400mil with 0.65mm pin pitch)
- Timing - Cycle Time
 - 5ns @ $CL = 3^{(1)}$
- Self Refresh
 - Standard

Marking

32M8
 16M16
 TG
 P
 -5B
 none

NOTE:

1. Supports PC3200 modules with 3-3-3 timing

General Description

The DDR400 SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 200 MHz ($t_{CK}=5ns$) with a peak data transfer rate of 400Mb/s/p. DDR400 continues to use the JEDEC standard SSTL_2 interface and the 2n-prefetch architecture.

The base Micron 256Mb data sheet provides full specifications and functionality unless specified herein. This addendum data sheet concentrates on the critical parameters and key differences required to support the enhanced DDR400 speeds.

Table 1: Configuration

ARCHITECTURE	32 MEG X 8	16 MEG X 16
Configuration	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	8K	8K
Row Addressing	8K (A0-A12)	8K (A0-A12)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	1K (A0-A9)	512 (A0-A8)

Table 2: Key Timing Parameters

SPEED GRADE	CLOCK RATE $CL = 3^{(1)}$	DATA-OUT WINDOW ²	ACCESS WINDOW	DQS-DQ SKEW
-5B	200 MHz	1.6ns	$\pm 700ps$	+400ps

NOTE:

1. $CL = CAS$ (Read) Latency
2. With a 50/50 clock duty cycle


Table 3: Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V _{DD} is applied and until CKE is first brought high. After CKE is brought high it becomes an SSTL_2 input only.
24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
47 20, 47	DM LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16 DM for DQ0-DQ7 and UDM is a DM for D08-D015. Pin 20 is a NC on x8.
26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29-31 32, 35, 36 37, 38, 39 40, 28, 41 42	A0, A1, A2 A3, A4, A5 A6, A7, A8 A9, A10, A11 A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
2, 5, 8 11, 56, 59 62, 65	DQ0-2 DQ3-5 DQ6-7	I/O	Data Input/Output. Data bus for x8
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0-DQ2 DQ3-DQ5 DQ6-DQ8 DQ9-DQ11 DQ12-DQ14 DQ15	I/O	Data Input/Output: Data bus for x16 (Pins 4, 7, 10, 13, 54, 57, 60, 63 are NC for the x8)


Table 3: Pin Descriptions (Continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
51 16, 51	DQS LDQS, UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. for the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 is a NC on x8.
14, 17, 25, 43, 53	NC	-	No Connect: These pins should be left unconnected.
19, 50	DNU	-	Do Not Use: Must float to minimize noise on Vref
3, 9, 15, 55, 61	V _{DDQ}	Supply	DQ Power Supply: +2.60V ±0.10V. Isolated on the die for improved noise immunity.
6, 12, 52, 58, 64	V _{SSQ}	Supply	DQ Ground. Isolated on the die for improved noise immunity.
1, 18, 33	V _{DD}	Supply	Power Supply: +2.60V ±0.10V.
4, 48, 66	V _{SS}	Supply	Ground.
49	V _{REF}	Supply	SSTL_2 reference voltage.



Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency should be set to 3 clocks, as shown in the CAS Latency Diagram and Mode Register Definition Diagram.

If a READ command is registered at clock edge n , and the latency is m clocks, the data will be available nominally coincident with clock edge $n + m$.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 4: CAS Latency (CL)

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)		
	CL = 3	CL = 2.5	CL = 2
-5B	133MHz ≤ f ≤ 200MHz	75MHz ≤ f ≤ 167MHz	75MHz ≤ f ≤ 133MHz

Figure 3: Mode Register Definition Diagram

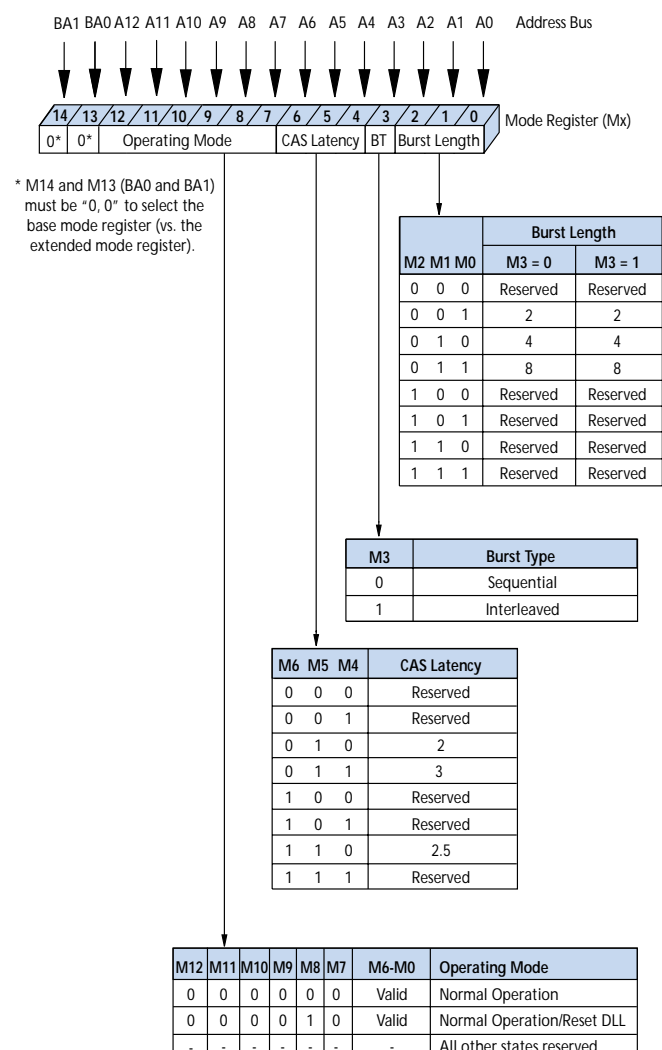
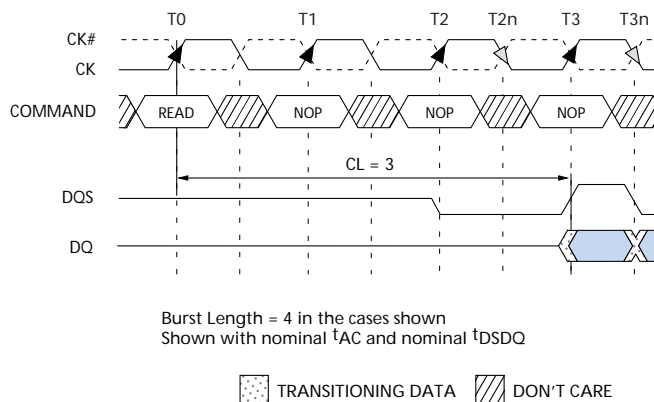


Figure 4: Example CAS Latency Diagram with CL=3





Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage	Relative to VSS	-1V to +3.6V
VDDQ Supply Voltage	Relative to VSS	-1V to +3.6V
VREF and Inputs Voltage	Relative to VSS	-1V to +3.6V
I/O Pins Voltage	Relative to VSS	-0.5V to VDDQ +0.5V
Operating Temperature, T _A (ambient).....		0°C to +70°C
Storage Temperature (plastic)		-55°C to +150°C
Power Dissipation.....		1W
Short Circuit Output Current		50mA

Table 5: DC Electrical Characteristics and Operating Conditions

0°C ≤ T_A ≤ +70°C; VDDQ = +2.6V ±0.1V, VDD = +2.6V ±0.1V

Notes: 1-5, 16, Refer to Base 256Mb Data Sheet, page 60-63 for all notes except 53 below.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	VDD	2.5	2.7	V	36, 41, 53
I/O Supply Voltage	VDDQ	2.5	2.7	V	36, 41, 44,53
I/O Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 44
I/O Termination Voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	7, 44
Input High (Logic 1) Voltage	V _{IH} (DC)	VREF + 0.15	VDD + 0.3	V	28
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.3	VREF - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ VDD, VREF Pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V _{OUT} ≤ VDDQ)	I _{OZ}	-5	5	μA	
OUTPUT LEVELS: Full drive option High Current (V _{OUT} = VDDQ - 0.373V, minimum VREF, minimum VTT)	I _{OH} I _{OL}	-16.8 -16.8	- -	mA mA	37, 39
OUTPUT LEVELS: Reduced drive option - x16 only High Current (V _{OUT} = VDDQ - 0.763V, minimum VREF, minimum VTT)	I _{OHR}	-9	-	mA	38, 39
Low Current (V _{OUT} = 0.763V, maximum VREF, maximum VTT)	I _{OLR}	9	-	mA	

Note 53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range of 2.6V ± 100mV.


Table 6: AC Input Operating Conditions
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$, $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$

Notes: 1-5, 16, Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.310$	-	V	14, 28, 40
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.310$	V	14, 28, 40
I/O Reference Voltage	$V_{REF(AC)}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	6

Table 7: Capacitance (x8 TSOP)

Note: 13; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQ0-DQ7	DC_{iO}	-	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{i1}	-	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{i2}	-	0.25	pF	29
Input/Output Capacitance: DQs, DQS, DM	C_{iO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{i1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{i2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{i3}	2.0	3.0	pF	

Table 8: Capacitance (x16 TSOP)

Note: 13; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQ0-DQ7, LDQS, LDM	DC_{iOL}	-	0.50	pF	24
Delta Input/Output Capacitance: DQ8-DQ15, UDQS, UDM	DC_{iOU}	-	0.50	pF	24
Delta Input Capacitance: Command and Address	DC_{i1}	-	0.50	pF	29
Delta Input Capacitance: CK, CK#	DC_{i2}	-	0.25	pF	29
Input/Output Capacitance: DQ, LDQS, UDQS, LDM, UDM	C_{iO}	4.0	5.0	pF	
Input Capacitance: Command and Address	C_{i1}	2.0	3.0	pF	
Input Capacitance: CK, CK#	C_{i2}	2.0	3.0	pF	
Input Capacitance: CKE	C_{i3}	2.0	3.0	pF	


Table 9: Electrical Characteristics and Recommended AC Operating Conditions
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$, $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$

Notes: 1-5, 14-17, 33, 46; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

AC CHARACTERISTICS		-5B				
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES	
Access window of DQs from CK/CK#	t_{AC}	-0.70	+0.70	ns		
CK high-level width	t_{CH}	0.45	0.55	t_{CK}	30	
CK low-level width	t_{CL}	0.45	0.55	t_{CK}	30	
Clock cycle time	CL=3	t_{CK}	5	7.5	ns	45, 52
	CL=2.5	t_{CK}	6	13	ns	42, 52
	CL=2	t_{CK}	7.5	13	ns	42, 52
DQ and DM input hold time relative to DQS	t_{DH}	0.40		ns	26, 31	
DQ and DM input setup time relative to DQS	t_{DS}	0.40		ns	26, 31	
DQ and DM input pulse width (for each input)	t_{DIPW}	1.75		ns	31	
Access window of DQS from CK/CK#	t_{DQSK}	-0.60	+0.60	ns		
DQS input high pulse width	t_{DQSH}	0.35		t_{CK}		
DQS input low pulse width	t_{DQSL}	0.35		t_{CK}		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}		0.40	ns	25, 26	
Write command to first DQS latching transition	t_{DQSS}	0.72	1.28	t_{CK}		
DQS falling edge to CK rising - setup time	t_{DSS}	0.2		t_{CK}		
DQS falling edge from CK rising - hold time	t_{DSH}	0.2		t_{CK}		
Half clock period	t_{HP}	t_{CH}, t_{CL}		ns	34	
Data-out high-impedance window from CK/CK#	t_{HZ}		+0.70	ns	18, 42	
Data-out low-impedance window from CK/CK#	t_{LZ}	-0.70		ns	18, 43	
Address and control input hold time (slew rate = 1V/ns)	t_{IH_F}	0.6		ns		
Address and control input setup time (slew rate = 1V/ns)	t_{IS_F}	0.6		ns		
Address and control input hold time (slew rate = 0.5V/ns)	t_{IH_S}	0.6		ns		
Address and control input setup time (slew rate = 0.5V/ns)	t_{IS_S}	0.6		ns		
Address and Control input pulse width (for each input)	t_{IPW}	2.2		ns		
LOAD MODE REGISTER command cycle time	t_{MRD}	10		ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	t_{HP} $-t_{QHS}$		ns	25, 26	
Data Hold Skew Factor	t_{QHS}		0.50	ns		
ACTIVE to READ with Auto precharge command	t_{RAP}	15		ns		
ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	ns	35	
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55		ns		
AUTO REFRESH command period	t_{RFC}	70		ns	50	
ACTIVE to READ or WRITE delay	t_{RCD}	15		ns		
PRECHARGE command period	t_{RP}	15		ns		
DQS read preamble	t_{RPRE}	0.9	1.1	t_{CK}	42	
DQS read postamble	t_{RPST}	0.4	0.6	t_{CK}		
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	10		ns		
DQS write preamble	t_{WPRE}	0.25		t_{CK}		
DQS write preamble setup time	t_{WPRES}	0		ns	20, 21	
DQS write postamble	t_{WPST}	0.4	0.6	t_{CK}	19	
Write recovery time	t_{WR}	15		ns		
Internal WRITE to READ command delay	t_{WTR}	2		t_{CK}		
Data valid output window (DVW)	N/A		$t_{QH} - t_{DQSQ}$	ns	25	
REFRESH to REFRESH command interval	t_{REFC}		70.3	μs	23	
Average periodic refresh interval	t_{REFI}		7.8	μs	23	
Terminating voltage delay to V_{DD}	t_{VTD}	0		ns		
Exit SELF REFRESH to non-READ command	t_{XSNR}	70		ns		
Exit SELF REFRESH to READ command	t_{XSRD}	200		t_{CK}		


Table 10: IDD Specifications and Conditions
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$, $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$

Notes: 1-5, 14-17, 33, 46, 53; Refer to Base 256Mb Data Sheet, page 60-63 for all notes.

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES	
		-5B (X8)	-5B (X16)			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	IDD0	135	135	mA	22, 48	
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 4; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$; Address and control inputs changing once per clock cycle	IDD1	170	185	mA	22, 48	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = (LOW)	IDD2P	4	4	mA	23, 32, 50	
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	IDD2F	60	60	mA	51	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW	IDD3P	40	40	mA	23, 32, 50	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	70	70	mA	22	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$	IDD4R	200	260	mA	22, 48	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	185	215	mA	22	
AUTO REFRESH BURST CURRENT:	$t_{RC} = t_{RFC}(\text{MIN})$	IDD5	260	260	mA	50
	$t_{RFC} = 7.8\mu\text{s}$,	IDD5A	6	6	mA	27, 50
SELF REFRESH CURRENT: CKE $\leq 0.2\text{V}$	Standard	IDD6	4	4	mA	11
	Low Power (L)	IDD6A	2	2	mA	11
OPERATING CURRENT: Four bank interleaving READS (Burst = 4) with auto precharge, $t_{RC} = \text{minimum } t_{RC} \text{ allowed}$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during Active READ, or WRITE commands	IDD7	470	510	mA	22, 49	



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